REMARKS

Claims 2-5, 7-9, 11-19 and 22-49 are pending in the above-referenced patent application. In this amendment, claims 2 and 44-45 have been amended. It is noted that claims 2 and 44-45 were amended to more clearly delineate intended subject matter, and not in light of cited references. Additionally, it is respectfully submitted that adequate support for the amendments to claims 2 and 44-45 may be found at least in the specification, figures, and claims as filed. Furthermore, the amendments to the claims introduce no new matter. It is respectfully requested that the Examiner enter the amendments to claims 2 and 44-45, and allow all pending claims to proceed to allowance.

Objections to the July 12, 2006 Amendment

In the Office Action, dated August 10, 2006, the Examiner objected to the amendment filed July 12, 2006 under 35 U.S.C. §132(a), alleging that the amendment introduces new matter into the disclosure. Specifically, the Examiner objects to the addition of the limitation "integrated multi-input adder" in claims 2, 17, 32 and 44. It is respectfully submitted that there is adequate support at least in the originally filed specification and figures to support the addition of the above-noted limitation. For example, support may be found at least in paragraphs [0032] and [0038] – [0043] and Figure 3. As just one example, quoting from paragraph [0043], "In addition to the hybrid Wallace tree 306, summing module 304 includes an m-input adder stage 318. ... In accordance with another implementation, i.e., when summing module is utilized in accordance with a multiply-accumulate operation, summing module generator 222 modifies the standard design rules to add another input and a series of registers within the summing module to accept feedback input of accumulator bits. That is, accumulator bits resulting during the multiplication process are fed back to registers (312) allocated within the (integrated) hybrid summing module." (emphasis supplied) It is respectfully submitted that no new matter is introduced by the July 12, 2006 amendments, and adequate support for the amendments is found at least in these cited portions of the specification, the figures, and the claims as filed.

Accordingly, it is respectfully requested that the Examiner withdraw this objection, and enter the amendments to the claims as presented in the July 12, 2006 amendment.

Claim Rejections

In the Office Action, the Examiner rejected claims 44-46 and 49 under 35 U.S.C 102(e) as being anticipated by Grisamore (U.S. Patent No. 6,535,901, hereinafter "Grisamore"); rejected claims 2-5, 7-9, 11-12, 17-19, 22-27 and 47-48 under 35 U.S.C 103(a) as being obvious over Grisamore and in view of Chang et al. (Hardware-efficient implementations for discrete function transforms using LUT-based FPGAs, Nov. 1999, IEEE Computers and Digital Techniques, pages 309-315, hereinafter "Chang"); rejected claims 13-16 and 28-31 under 35 U.S.C 103(a) as being obvious over Grisamore in view of Chang, and further in view of Fang et al. ("A hierarchical function structuring and partitioning approach for multiple-FPGA implementations, Oct. 1997, IEEE Computer-Aided Design of Integrated Circuits and Systems, pages 1188-1195, hereinafter "Fang"); rejected claims 32, 36-38 and 42-43 are rejected under 35 U.S.C 103(a) and being obvious over Grisamore in view of Greenberger (U.S. Patent No. 6,411,979, hereinafter "Greenberger"); rejected claims 33-35 are rejected under 35 U.S.C 103(a) and being obvious over Grisamore in view of Greenberger, in view of Chang; claims 39-41 are rejected under 35 U.S.C 103(a) and being obvious over Grisamore in view of Greenberger, in view of Chang, and in further view of Fang. These rejections are respectfully traversed.

Claim Rejection – 102(e)

The Examiner has rejected claims 44-46 and 49 under 35 U.S.C 102(e) as being anticipated by Grisamore. This rejection is respectfully traversed. Assignee respectfully submits that Grisamore does not set forth each and every element of the 44-46 and 49, and accordingly, contrary to the Examiner's assertion, the claims are not anticipated by Grisamore under 35 U.S.C. 102(e). As just an example, Grisamore does not show or describe "a summing module generator, said summing module generator being adapted to: receive input terms; perform bit-wise analysis of the input terms; and dynamically configure a summing module, wherein the summing module, as configured, comprises: a hybrid

Wallace tree comprising one or more elements, wherein the elements comprise one or more adders having one or more associated registers and one or more additional registers, wherein the Wallace tree comprises a reduced number of elements to perform summing operations on the one or more input terms; and an integrated multi-input adder configured to combine summation results produced by the configured summing module." As recited in claim 44.

Grisamore clearly describes passing partial products from the reduction tree module 18 to an adder 14 which is external from the reduction tree module, and is therefore not integrated with the reduction tree module. See, for example, col 3:28 – col 3:30 and Figure 1 of Grisamore. Accordingly, because adder 14 of Grisamore is clearly not an integrated multi-input adder, as set forth in claim 44, Grisamore fails to disclose each and every element of the rejected claims. Therefore, a sufficient showing of anticipation has not been established, and claim 44 is in a condition for allowance. Additionally, claims 45-46 and 49 depend from and include all limitations of claim 44, and are, therefore, in a condition for allowance on at least the same basis.

It is noted that many other bases for traversing the rejection could be provided, but Assignee believes that this ground is sufficient. Assignee respectfully submits that because Grisamore fails to disclose each and every element of the rejected claims, a sufficient showing of anticipation has not been established, and all pending claims are in a condition for allowance. It is respectfully requested that the Examiner withdraw his rejections of these claims.

Claim Rejections – 35 U.S.C §103(a)

Grisamore v Chang

The Examiner has rejected claims 2-5, 7-9, 11-12, 17-19, 22-27 and 47-48 under 35 U.S.C 103(a) as being obvious over Grisamore and in view of Chang. This rejection is respectfully traversed. It is respectfully submitted that claims 2-5, 7-9, 11-12, 17-19, 22-27 and 47-48 are not rendered obvious by a combination of Grisamore and Chang. For example, any combination of Grisamore and Chang would still not teach or suggest all the claim limitations. However, Assignee does not by this argument accept that the combination is proper; rather, while Assignee asserts that the combination is

improper, Assignee further asserts that even if the combination were proper, the combination would still fail to provide all the elements of the rejected claims.

Assignee begins with claim 2. The Examiner already concedes that Grisamore is lacking one or more elements of the rejected claims. For example, the Examiner states: "Grisamore does not disclose a dedicated logic device couple[d] to the summing module. However, Chang et al. disclose[s] the series of Boolean function generators as a summing module is coupled with a dedicated logic device comprising an FPGA" However, even if the successful combination of Grisamore and Chang were made, although, as stated previously, Assignee has serious doubts concerning the ability to do so, the resultant combination or any of the other alleged combinations would still not teach or suggest all the elements of claim 2. As just an example, Chang is directed generally toward LUT based FPGAs, and does not teach or suggest "a summing module generator coupled with the dedicated logic device, wherein the summing module generator is adapted to structure the dedicated logic device to implement a multi-stage summing module comprising one or more full-adders and associated registers, half-adders and associated registers, and single registers, wherein the summing module is adapted to produce intermediate summation results by combining the multiple input terms according to a pipelined reduction pattern, wherein the summing module generator is further adapted to implement an integrated multi-input adder into the summing module, wherein the integrated multi-input adder includes a plurality of inputs, wherein at least a portion of the plurality of inputs are adapted to receive feedback input of accumulator bits from one or more of the full-adders and associated registers, half-adders and associated registers, and single registers of the summing module and further adapted to produce a final sum of the multiple input terms by combining the intermediate summation results." As noted above, Chang describes LUT based FPGAs in general terms, but does not teach or suggest a dedicated logic device comprising an integrated multi-input adder. The portion of Chang cited by the Examiner describes an implementation of an FPGA. However, there is no description throughout Chang of a dedicated logic device comprising an integrated multi-input adder, and, as noted above, Grisamore does not cure these deficiencies. For example, as mentioned previously, Grisamore clearly describes passing partial products from a reduction tree module 18 to an adder 14 which is external

with respect to the reduction tree module, and therefore is not integrated with the reduction tree module. See, for example, col 3:28 – col 3:30 and Figure 1 of Grisamore.

It is respectfully submitted, therefore, that at least one element of claim 2 is absent from the cited art, and any alleged combination would still not teach or suggest all of the elements of claim 2. Additionally, claims 3-5, 7-9, 11-12, 17-19, 22-27 and 47-48 distinguish from the cited art for at least the same reasons. It is therefore respectfully requested that the Examiner withdraw his rejection of these claims, and allow these claims to proceed to allowance.

Grisamore v Chang v Fang

The Examiner has rejected claims 13-16 and 28-31 under 35 U.S.C 103(a) as being obvious over Grisamore in view of Chang, and further in view of Fang. This rejection by the Examiner is respectfully traversed. The Examiner already concedes that Grisamore and Chang are lacking one or more elements of the rejected claims. For example, the Examiner states "Grisamore in view of Chang do not disclose in Figures 1, 4-5 and 7 a controller or a logic control module dynamically structures the atomic elements of the dedicated logic device. However, Fang et al. disclose in Figure 3 a controller or a logic control module dynamically ... structures the atomic elements of the dedicated logic device." However, even if the successful combination of Grisamore, Chang and Fang were made, although, as stated previously, Assignee has serious doubts concerning the ability to do so, the resultant combination or any of the other alleged combinations would still not teach or suggest the elements of the rejected claims. Fang is directed toward structuring and partitioning of FPGA implementations. The cited passage recites hierarchical structuring of an FPGA implementation, and does not cure the deficiencies of Grisamore and Chang, noted above. For example, none of Grisamore, Chang nor Fang teach or suggest a summing module generator "wherein the summing module generator is further adapted to implement an integrated multi-input adder into the summing module, wherein the integrated multi-input adder includes a plurality of inputs, wherein at least a portion of the plurality of inputs are adapted to receive feedback input of accumulator bits from one or more of the full-adders and associated registers, half-adders and associated registers, and single registers of the summing module

and further adapted to produce a final sum of the multiple input terms by combining the intermediate summation results.", as recited in claim 2, from which claim 13 depends. Therefore, any resultant combination of Grisamore with Chang and/or Fang would not produce the elements of claim 13. Claims 14-16 and 28-31 either depend from or include limitations similar to those of claim 13, and, accordingly, are in a condition for allowance on at least the same basis.

It is respectfully submitted, therefore, that at least one element of claims 13-16 and 28-31 is absent from the cited art, and any alleged combination would still not teach or suggest all of the elements of the rejected claims. It is therefore respectfully requested that the Examiner withdraw his rejection of these claims.

Grisamore v Greenburger v Chang

The Examiner has rejected claims 32, 36-38, and 42-43 under 35 U.S.C 103(a) as being obvious over Grisamore in view of Greenburger, claims 33-35 under 35 U.S.C 103(a) as being obvious over Grisamore in view of Greenburger, further in view of Chang, and claims 39-41 under 35 U.S.C 103(a) as being obvious over Grisamore in view of Greenburger, in further view of Chang, in further view of Fang. These rejections are respectfully traversed.

Beginning with claim 32, the Examiner already concedes that Grisamore is lacking one or more elements of the rejected claims. For example, the Examiner states: "Grisamore does not implicitly disclose two paths one for a real component branch, inverting certain partial produces and passing the inverted and non-inverted partial products and one for an imaginary component branch, passing the partial products to a multi-stage series of Boolean function generators simultaneously." It is respectfully submitted that even if the successful combination of Grisamore with Greenburger, and/or Chang and/or Fang were made, although, as stated previously, Assignee has serious doubts concerning the ability to do so, the resultant combination or any of the other alleged combinations would still not teach or suggest the elements of the rejected claims.

Greenburger is directed toward a complex number multiplier circuit, and does not cure the deficiencies of Grisamore and/or Chang and/or Fang, noted above. For example, neither Chang, Fang

nor Greenburger teach or suggest at least "simultaneously passing the partial products from the two or more input terms to a multi-stage series of Boolean function generators that implements one or more full-adders and associated registers, half-adders and associated registers, and single registers to produce intermediate summation results by combining the partial products; determining the structure of the Boolean function generators based, at least in part, on one or more attributes of the input terms; receiving in both branches accumulator bits over a feedback path, wherein the accumulator bits are respectively provided to an integrated multi-input adder; and adding the intermediate summation results with the accumulator bits for each branch to produce a final real-component sum and a final imaginary-component sum.", as recited in claim 32. Additionally, as alluded to previously, none of Grisamore, Fang or Chang teach or suggest "an integrated multi-input adder", as recited in claim 32, and Greenburger does not teach or suggest any implementation of "an integrated multi-input adder". Therefore, any resultant combination of Grisamore and Chang, Fang nor Greenburger would not produce the elements of claim 32, as amended. Claims 33-43 depend from and include all limitations of claim 32, and distinguish from the cited art at least on the same basis as claim 32.

It is respectfully submitted, therefore, that at least one element of claims 32-43 is absent from the cited art, and any alleged combination would still not teach or suggest all of the elements of the rejected claims. It is therefore respectfully requested that the Examiner withdraw his rejection of these claims.

Assignee respectfully submits that, for at least the reasons presented above, the pending claims are not rendered obvious in light of cited references, and, therefore, the rejected claims are in a condition for allowance. It is noted that many other bases for traversing these rejections could be provided, but Assignee believes that this ground is sufficient. It is respectfully requested that the Examiner withdraw this rejections of these claims.

CONCLUSION

In view of the foregoing, it is respectfully submitted that all claims presented are in a condition for allowance, and early allowance of all claims pending in the application is respectfully requested. If the Examiner has any questions, he is invited to contact the undersigned at (503) 439-6500.

Please charge any shortages and credit any overcharges of any fees required for this submission to Deposit Account number 50-3703.

Respectfully submitted,

Dated: February 12, 2007

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